REMARKS

Applicants appreciate the thorough examination of the present application as evidenced by the Final Office Action of January 7, 2009 (hereinafter "Final Action"). Applicants have amended the claims as set out above and, therefore, respectfully request reconsideration and allowance of the pending claims for at least the reasons discussed herein.

The Section 102 Rejections

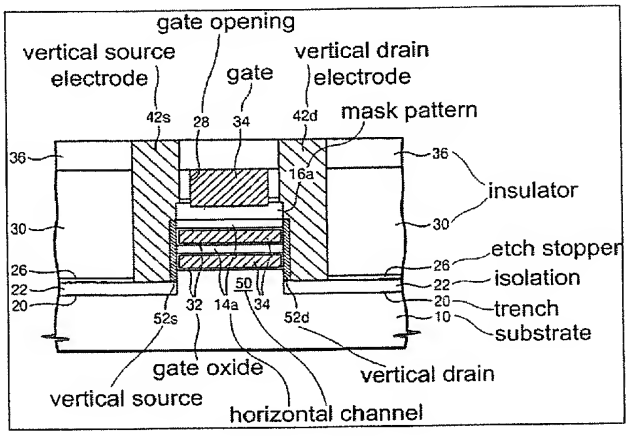
Claims 12-19 and 30 stand rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 5,583,362 to Maegawa (hereinafter "Maegawa"). *See* Final Action, page 3. Applicants respectfully submit that many of the recitations of these claims are neither disclosed nor suggested by Maegawa. For example, amended Claim 12 recites:

> A method of forming a unit cell of a metal oxide semiconductor (MOS) transistor, comprising:
>
> forming a MOS transistor on an integrated circuit substrate including an isolation layer and an active region higher than the isolation layer, **the MOS transistor having a pair of junctions consisting of a vertical source region and a vertical drain region on the isolation layer**, and a plurality of gates on the active region, the plurality of gates being stacked between the vertical source region and the vertical drain region;
>
> forming a horizontal channel between the vertical source region and the vertical drain region, the horizontal channel including at least two horizontal channel regions formed in spaced apart patterns, wherein the pair of junctions are vertically formed to cover the sides of the active region in other patterns adjacent to sides of the spaced apart patterns so that the pair of vertical junctions contact the sides of the at least two spaced apart horizontal channel regions; and
>
> forming a vertical source electrode electrically connected to the vertical source region and a vertical drain electrode electrically connected to the vertical drain region, **wherein the vertical source and drain electrodes are formed on the isolation layer so that the vertical source and drain electrodes contact sides of the vertical source and drain regions, respectively**.

Applicants respectfully submit that at least the highlighted recitations of amended independent Claim 12 are neither disclosed nor suggested by Maegawa for at least the reasons discussed herein.

Responsive to Applicants' arguments, the Final Action states that Maegawa inherently discloses a pair of vertical source and drain regions which are implicitly disclosed by figure 30 similar to the present invention because "'region[s]' is a broad term which does not exclude the plurality of vertically stacked source/drain junctions." *See* Final Action, page 2.

Applicants disagree. In particular, Claim 12 recites a single vertical source region and a single vertical drain region. Maegawa discusses a plurality of vertically stacked source regions and a plurality of vertically stacked drain regions. Furthermore, Claim 12 recites that the vertical source and drain electrodes are formed on the isolation layer so that the vertical source and drain electrodes contact sides of the vertical source and drain regions, respectively. This feature of the present invention is clearly illustrated in the figure set out below. Specifically, a vertical source electrode 42s directly contacts a side of the vertical source region 52s and a vertical drain electrode 42d directly contacts a side of the vertical drain region 52d. The vertical source/drain electrodes 42s and 52s are formed on the isolation layer 22. This structure can increase contact area between the vertical source/drain electrodes 42s and 42d and the vertical source/drain regions 52s and 52d. Also, the isolation layer 22 provided between the vertical source/drain electrodes 42s, 42d and the integrated circuit substrate 10 can reduce leakage current from the vertical source/drain electrodes 42s, 42d into the integrated circuit substrate 10.



Finally, the Final Action points to column 8, lines 65-67 of Maegawa as teachings a vertical source electrode electrically connected to the vertical source region and a vertical drain electrode electrically connected to the vertical drain region as recited in Claim 12. *See* Final Action, page 5. Applicants can find no discussion related to vertical source/drain electrodes in the cited portion of Maegawa. Accordingly, for at least the reasons discussed herein, Applicants respectfully submit that Maegawa does not anticipate Claim 12. Thus, Applicants respectfully submit that Claim 12 and the claims that depend therefrom are patentable over Maegawa.

Amended independent Claim 30 recites:

> A method of forming a unit cell of a metal oxide semiconductor (MOS) transistor, comprising:
> forming a horizontal channel between **a vertical source region and a vertical drain region**, the horizontal channel including at least two horizontal channel regions formed in spaced apart patterns;
> forming the vertical source region and the vertical drain region in other patterns at one side of the spaced apart patterns, respectively; and
> **forming a vertical source electrode contacted to a side of the vertical source region and a vertical drain electrode contacted to a side of the vertical drain region**.

Applicants respectfully submit that the highlighted portions of independent Claim 30 are patentable over Maegawa for at least reasons similar to those discussed above with respect to Claim 12.

The Section 103 Rejections

Claims 20-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Maegawa in further view of United States Patent No. 6,420,758 to Nakajima (hereinafter "Nakajima"). *See* Final Action, page 8. Applicants respectfully submit that many of the recitations of these claims are neither disclosed nor suggested by the cited combination. For example, amended Claim 23 recites:

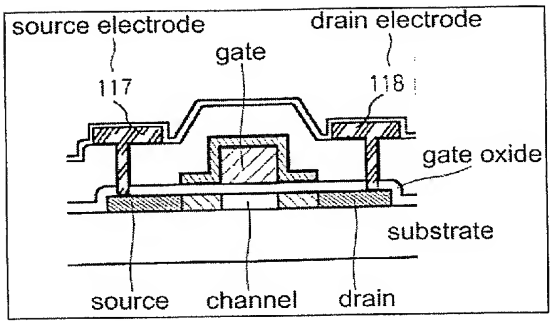
> A method of fabricating a transistor comprising:
> forming a trench region on an integrated circuit substrate to define an active region;
> forming a stacked structure including at least one set of first epitaxial patterns and second epitaxial patterns on the active region;
> forming a first insulation pattern on a floor of the trench;
> growing a third epitaxial layer on sidewalls of at least one set of first and second epitaxial patterns;
> forming a second insulation pattern on a surface of the integrated circuit substrate, the second insulation pattern defining a gate opening that exposes at least a portion of the third epitaxial layer;
> removing the third epitaxial layer in the gate opening to expose the set of at least one first and second epitaxial patterns;
> selectively etching the first epitaxial patterns of the set of at least one first and second epitaxial patterns to form a horizontal channel region having a plurality of spaced apart channel layers;
> forming a gate oxide layer on a surface of channel layers;
> forming a gate pattern on the horizontal channel and in gap regions between the channel layers and the gate opening; and

forming a vertical source electrode and a vertical drain electrode on the first insulation pattern penetrating the second insulation pattern to be connected to the third epitaxial layer.

Applicants respectfully submit that at least the highlighted recitations of amended independent Claim 23 are neither disclosed nor suggested by the cited combination for at least the reasons discussed herein.

The Final Action admits that Maegawa does not explicitly disclose the source/drain electrodes connected to the vertical source/drain regions. *See* Final Action, page 8. However, the Final Action states that it is notoriously well known to extend source/drain electrodes to make electrical contact with the source/drain regions and points to Nakajima as teaching source/drain electrodes to the source/drain regions. The Final Action concludes that the combination of Maegawa and Nakajima would show the vertical source/drain electrodes connected to the vertical source/drain regions as recited in Claim 23. Applicants respectfully disagree.

In particular, as illustrated in the Figure of Nakajima reproduced below, Nakajima teaches that the vertical source/drain electrodes 117 and 118 are connected to the source/drain regions, the vertical source/drain electrodes 117, 118 are formed on upper surfaces of the source region (not on the isolation layer) so that the vertical source/drain electrodes 117, 118 contact the upper surfaces (not sides) of the source/drain regions, respectively. In stark contrast, Claim 23 recites "forming a vertical source electrode and a vertical drain electrode on the first insulation pattern penetrating the second insulation pattern to be connected to the third epitaxial layer." The combination of Maegawa and Nakajima discusses forming the vertical source/drain electrodes on the source/drains regions so that the vertical source/drain electrodes contact upper surfaces of the source/drain regions, respectively. Accordingly, the combination of Maegawa and Nakajima fails to disclose or suggested the highlighted recitations of Claim 23 for at least these reasons. Thus, Applicants respectfully submit that independent Claim 23 and the claims that depend therefrom are patentable over the cited combination for at least these reasons.



CONCLUSION

Applicants respectfully submit that pending claims are in condition for allowance, which is respectfully requested in due course. Favorable reconsideration of this application is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,

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CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on March 25, 2009.

Candi L. Riggs